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PATENT
YOR920000192 IBM-2282

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Alan Gene Gara
Serial Number	:	~~09/799,038~~ 09/779,038
Filing Date	:	February 8, 2001
Examiner	:	Qutbudden Ghulamali
Group Art Unit	:	2637
For	:	BINARY DATA TRANSMISSION ON A SINGLE TRANSMISSION CHANNEL

TO: The Honorable Commissioner of Patents
and Trademarks
Post Office Box 1450
Alexandria, VA 22313-1450

PETITION TO REVIVE ABANDONED APPLICATION

The undersigned, as Attorney of Record, submits this petition to request that a holding of Abandonment of the above-entitled application be withdrawn. This Petition is submitted despite the fact that there has been no specific Notice of Abandonment sent to Applicant by the United States Patent and Trademark Office ("USPTO").

An Official Action in this case dated July 30, 2004, was sent by the Examiner to Applicant. The Official Action required minor changes to Figure 2 of the drawings, rejected some claims and allowed claims 5 and 13 subject to inclusion of the base claim and any intervening claims therein.

Applicant's Attorney prepared an amendment in compliance with what the Examiner had

suggested in the Official Action with the expectation that Claims 5 and 13 would be issued in amended form. He filed a written response to the Official Action on October 28, 2004 by telefax sent to (703) 872-9306 which at the time was the correct fax number for filing submissions with the USPTO. A copy of the Amendment so transmitted on October 28, 2004 is enclosed as Appendix A. An enlarged segment of the page containing the Certificate of Mailing (Transmission) is enclosed as Appendix B.

Immediately after Appendix A (and inherently, Appendix B) was filed, Applicant's Attorney did not receive an auto-reply facsimile transmission confirmation of receipt form. At that time, it was assumed that the receipt was not transmitted by return fax because there was a backlog of receipts to be sent out from the automatic return system in the USPTO.

Applicant's Attorney obtained corrected drawings and filed same using the U.S. Postal Service on October 29, 2004.

In May of this year, as part of a routine status checkup of cases within his docket, Applicant's Attorney noted that there was no communication received from the USPTO with respect to this case. Applicant's attorney called the Examiner in charge of this application to inquired why no further communication had been received and the Examiner advised Applicant's attorney that no response (i.e., Appendix A) amending the claims had been received; but the USPTO had received the amended drawings. Upon receiving that information, Applicant's Attorney submitted a copy of the amended that had been transmitted on October 28, 2004. This later copy of appendix A was telefaxed on May 27, 2005.

On August 9, 2005 Applicant received an Official Action in which the Examiner did not declare or hold that the application was abandoned, but rather stated that *"...The Application will become abandoned unless applicant obtains an extension of the period for reply set in the above noted Official Action"...*

Upon receipt of the Official Action, Applicant's Attorney immediately called the Examiner in charge of the case to again discuss the situation.

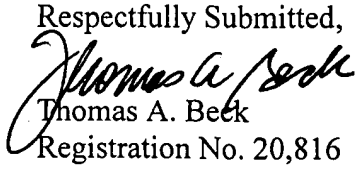
After several conversations with the Examiner, Applicant's Attorney consulted with Mr. Douglas Wood of the USPTO who advised that the instant petition should be made in the form of a Petition to Withdraw a Holding of Abandonment as the case was abandoned as a matter of law, even though no specific document has been issued that specifically states that the case is held to be abandoned. By using such a title designation, the Examiner can consider the case and act promptly on the request, thus keeping it within the Group.

Applicant respectfully requests that the holding of "Abandonment" in this application be withdrawn since Applicant did submit the Appendix A amendment response timely, i.e. prior to October 30, 2004. Appendix B supports this assertion. Applicant's Attorney states unequivocally that he filed the response with the USPTO by fax on the date, both as stated in Appendix A

The courtesy extended to Applicant's Attorney by Examiner Ghulamali and Mr Wood during the many telephone conferences on this case is gratefully acknowledged.

As anecdotal evidence in this matter, Applicant's Attorney declares that in the past three days he has submitted papers to the USPTO to both the new fax number and the old one, and at no time has he received a confirmation of the receipt of the transmission of any of these documents so sent. Thus inferences of problems within the telefacsimile system of the USPTO can properly be drawn. Applicant will mail a duplicate copy of this Petition to insure that it is received.

Respectfully Submitted,



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I hereby certify that this paper is being telefaxed to (571) 273-8300 on the date indicated below and is addressed to Commissioner of Patents & Trademarks, Post Office Box 1450, Alexandria, VA 22313-1450.

and (703) 872-9306

Signature: Thomas A. Beck Date: September 2, 2005

Name: Thomas A. Beck

Mailed September 2, 2005

Thomas A Beck

PATENT
Attorney Docket YOR20000548US2
IBM-282

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Alan Gene Gara
Serial Number	:	09/779,038
Filing Date	:	February 8, 2001
Examiner	:	Qutbuddin Ghulmali
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To: The Honorable Commissioner of
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Post Office Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Official Action dated July 30, 2004 please amend the claims in the above-identified application as follows:

CLAIMS

APPENDIX A

1. (Currently Amended) In the transmission of clocked time binary information signals with respect to a single reference level in a single information channel where said binary information signals are positioned between beginning and end phase shift signals,

an improvement for extraction of said phase shift signals comprising in combination:

means for arranging said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voiltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels.

2. (Previously presented) The improvement of claim 1 wherein said means for arranging said binary information signals in serial relation to said first, second and third voltage levels includes a three level driver.

3. (Currently Amended) The improvement of claim ~~1~~ 2 wherein said means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal that is greater than a low threshold that is less than the transition between said first and said second of said voltage levels and is less than a high threshold that is greater than the transition between said second and said thrid voltage levels as one reference and said low threshold as the other reference level.

4. (Previously presented) The improvement of claim ~~1~~ 3 wherein said means for producing a new signal includes means for reflecting "current" and "previous" data in relating said new signal to said clocked time.

5. (Previously Presented) The improvement of claim 4 wherein said means for electing "current" and "previous" data is a look-up table with said "previous" data provided from said "current" data with a one clock time cycle delay.

6. (Currently Amended) Clocked time binary information processing comprising:
the arrangement of said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

~~the~~ producing ~~of~~ a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voiltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels and the processing of said new signal in a differential amplifier between said high and said low threshold values.

7. (Curently Amended) The clocked time binary information processing of claim 6 including ~~the~~ an additional step of further position processing of said new signal with respect to said clocked time.

8. (Curently Amended) The clocked time binary information processing of claim 7 wherein said additional step is a signal positioning of said new signal at the leading edge of said clocked time.

9. (Currently Amended) The removal of clock timing information and signal reshaping in binary data comprising the steps of :

arranging said binary data in serial binary bits,

passing each bit in relation to first, second and third voltage levels, wherein each binary bit signal extends into two of said voltage levels such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

producing a new signal for each bit that is within an amplitude range that is greater than a low threshold value that is less than a transition value between said first and said second of said voltage levels and is less than a high threshold value greater than the transition value between said second and said third voltage levels, and,

positioning said new signal in relation to the leading edge of the next clock timing signal.

10. (Currently Amended) Data transmission apparatus for the transmission of binary data bits between first and second nodes, comprising in combination:

an input stage operable to receive a binary information signal at a first transmission node, said input stage being adapted to deliver a three voltage level driver signal ~~voltage~~ at an intermediate circuit node,

said three voltage level driver signal having serially, in a first clock cycle increment, a first voltage level corresponding to the system reference voltage,

in a second clock cycle increment, a second and intermediate~~[,]~~ voltage level and,

in a third clock cycle increment corresponding to a third and highest voltage level,

a comparator stage wherein said three level driver signal is compared in separate parallel first and second reference voltage comparison amplifiers each having said three level driver signal introduced at one input thereto;

a first reference voltage comparison amplifier having introduced at the remaining input a low threshold voltage that is higher than said reference voltage and is less than said intermediate voltage, and,

a second reference voltage comparison amplifier having introduced at the remaining input a high threshold voltage that is higher than said intermediate voltage and is less than said third voltage; and

a binary information signal reconstruction stage responsive to output signals from said first and second comparison amplifiers ~~ans~~ and adapted to establish the shape of an output binary bit signal;

such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape.

11. The data transmission apparatus of claim 10 wherein said reconstruction stage includes delay means to position said output signal with respect to a clock for said data transmission system.

12. (Previously presented) The data transmission apparatus of claim 11 wherein said reconstruction stage includes variable delay means to position said output signal within a window established by said clock for said data transmission system.

13. (Previously presented) The data transmission apparatus of claim 12 wherein said reconstruction stage includes bistable circuit means establishing output signal turn-on.

14. (Presently Amended) The data transmission apparatus of claim ~~12~~ 13 wherein said reconstruction stage produces a new signal, the magnitude of which is within an amplitude range that is greater than a low threshold value that is less than an intermediate voltage value that is between said first and said second of said voltage levels, and is less than a high threshold value that is greater than said intermediate voltage, and, positioning said new signal in relation to the leading edge of the next clock timing signal.

15. (New) In the transmission of clocked time binary information signals with respect to a single reference level in a single information channel where said binary information signals are positioned between beginning and end phase shift signals,

an improvement for extraction of said phase shift signals comprising in combination:

means for arranging said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels, said means including means for reflecting "current" and "previous" data in relating said new signal to said clocked time; and said means for reflecting "current" and "previous" data is a look-up table with said "previous" data provided from said "current" data with a one clock time cycle delay.

16 (New) Data transmission apparatus for the transmission of binary data bits between first and second nodes, comprising in combination:

an input stage operable to receive a binary information signal at a first transmission node, said input stage being adapted to deliver a three voltage level driver signal at an intermediate circuit node,

said three voltage level driver signal having serially, in a first clock cycle increment, a first voltage level corresponding to the system reference voltage,

in a second clock cycle increment, a second and intermediate voltage level and,

in a third clock cycle increment corresponding to a third and highest voltage level,

a comparator stage wherein said three level driver signal is compared in separate parallel first and second reference voltage comparison amplifiers each having said three level driver signal introduced at one input thereto;

a first reference voltage comparison amplifier having introduced at the remaining input a low threshold voltage that is higher than said reference voltage and is less than said intermediate voltage, and,

a second reference voltage comparison amplifier having introduced at the remaining input a high threshold voltage that is higher than said intermediate voltage and is less than said third voltage; and

a binary information signal reconstruction stage responsive to output signals from said first and second comparison amplifiers and adapted to establish the shape of an output binary bit signal; such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape;

said binary information reconstruction stage includes: (a) delay means to position said output signal with respect to a clock for said data transmission system; (b) variable delay means to position said output signal within a window established by said clock for said data transmission system and (c) bistable circuit means establishing output signal turn-on.

REMARKS

The Examiner is respectfully requested to reconsider his rejection of Claims 1 - 13 under 35 U.S.C. § 102(b) as being anticipated by Davies, et al. (U.S. Patent 5,255,287). Applicant has modified claims 1 - 14 to distinguish them over the Davies, et al. reference. All of the rejections of claims 1 - 13 are covered in this response in a single discussion. It is pointed out to the Examiner that there was no discussion of Claim 14 in the Official Action.

Davies, et al. do teach a method for transmitting and receiving digital (binary) data. This is where the similarity terminates. Davies, et al. However do not dislcose trransitions every cycle so their invention is directed toward a totally different objective.

Applicant has distinguished his invention from Davies, et al. By including in all independent claims the language that recites that there is a binary information signal reconstruction stage which is responsive to output signals from the first and second comparison amplifiers and adapted to establish the shape of an output binary bit signal, (Page 3, penultimate paragraph) such that *"there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape."*

If there are any charges associated with the filing of this response, the Commissioner is authorized to charge deposit account 50-0510.

A "Change of Correspondence Address" on behalf of the undersigned is enclosed. Please address all further correspondence to the undersigned at the address listed below.

Respectfully Submitted,

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I hereby certify that this paper is being telefaxed to (703) 872-9306 on the date indicated below addressed to the Commissioner of Patents and Trademarks, Post Office Box 1450, Alexandria, VA 22313-1450

Signature _____ Date: October 28, 2004
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Signature _____ Date: October 28, 2004
Thomas A. Beck

APPENDIX B